OMAP35xx Applications Processor Introduction

Texas Instruments OMAP™ Family of Products

Technical Reference Manual

Literature Number: SPRUFF1
February 2008

TEXAS INSTRUMENTS

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Introduction

This chapter introduces the features, supporting subsystems, and architecture of the OMAP35xx high-performance applications processors.

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1.1 Overview

The OMAP35xx family of high-performance, applications processors are based on the enhanced OMAP™ 3 architecture and are integrated on TI's advanced 65-nm process technology.

Note: The OMAP 3 architecture is configured with different sets of features in different devices. This technical reference manual details all of the features available in current and future OMAP35xx devices. Some features may not be available or supported in your particular device. For more information, see Section 1.5, *OMAP35xx Family* and your device-specific data manual.

The architecture is designed to provide best-in-class video, image, and graphics processing sufficient to support the following:

- Streaming video
- 2D/3D mobile gaming
- Video conferencing
- High-resolution still image
- Video capture in 2.5G wireless terminals, 3G wireless terminals, and rich multimedia-featured handsets, and high-performance personal digital assistants (PDAs).

This OMAP device also features the M-Shield™ mobile security technology to enable more secure e-commerce applications and the replay of copyright-protected digital media content.

Security features integrated on the devices support applications designed for:

- Protection against malicious attacks
- M-commerce
- Content protection for recordable media (CPRM)
- Digital rights management (DRM)

High-security (HS) devices rely on a security scheme based on hardware mechanisms and a secure read-only memory (ROM) code, ensuring that only trusted code can access the secure resources. These resources are in specific regions of memories as well as in peripherals, hardware cryptographic accelerators, and eFuse keys. General-purpose (GP) devices do not include a security feature.

Note: This technical reference manual focuses only on general-purpose (GP) devices. To determine if a high-security (HS) version of your device is available and for more information on HS devices, see Section 1.5, *OMAP35xx Family* , and your device-specific data manual.

The device supports high-level operating systems (OSs), such as:

- Windows CE
- Symbian OS
- Linux
- Palm OS

This OMAP device includes state-of-the-art power-management techniques required for high-performance mobile products.

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8™ microprocessor
- IVA2.2 subsystem with a C64x+ digital signal processor (DSP) core
- SGX530 subsystem for 2D and 3D graphics acceleration to support display and gaming effects

Note: IVA2.2 and SGX are not available on all devices. See Section 1.5, *OMAP35xx Family*, for more information on available features.

- Camera image signal processor (ISP) that supports multiple formats and interfacing options connected to a wide variety of image sensors
- Display subsystem with a wide variety of features for multiple concurrent image manipulation, and a programmable interface supporting a wide variety of displays. The display subsystem also supports NTSC/PAL video out.
- Level 3 (L3) and level 4 (L4) interconnects that provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals

The device also offers:

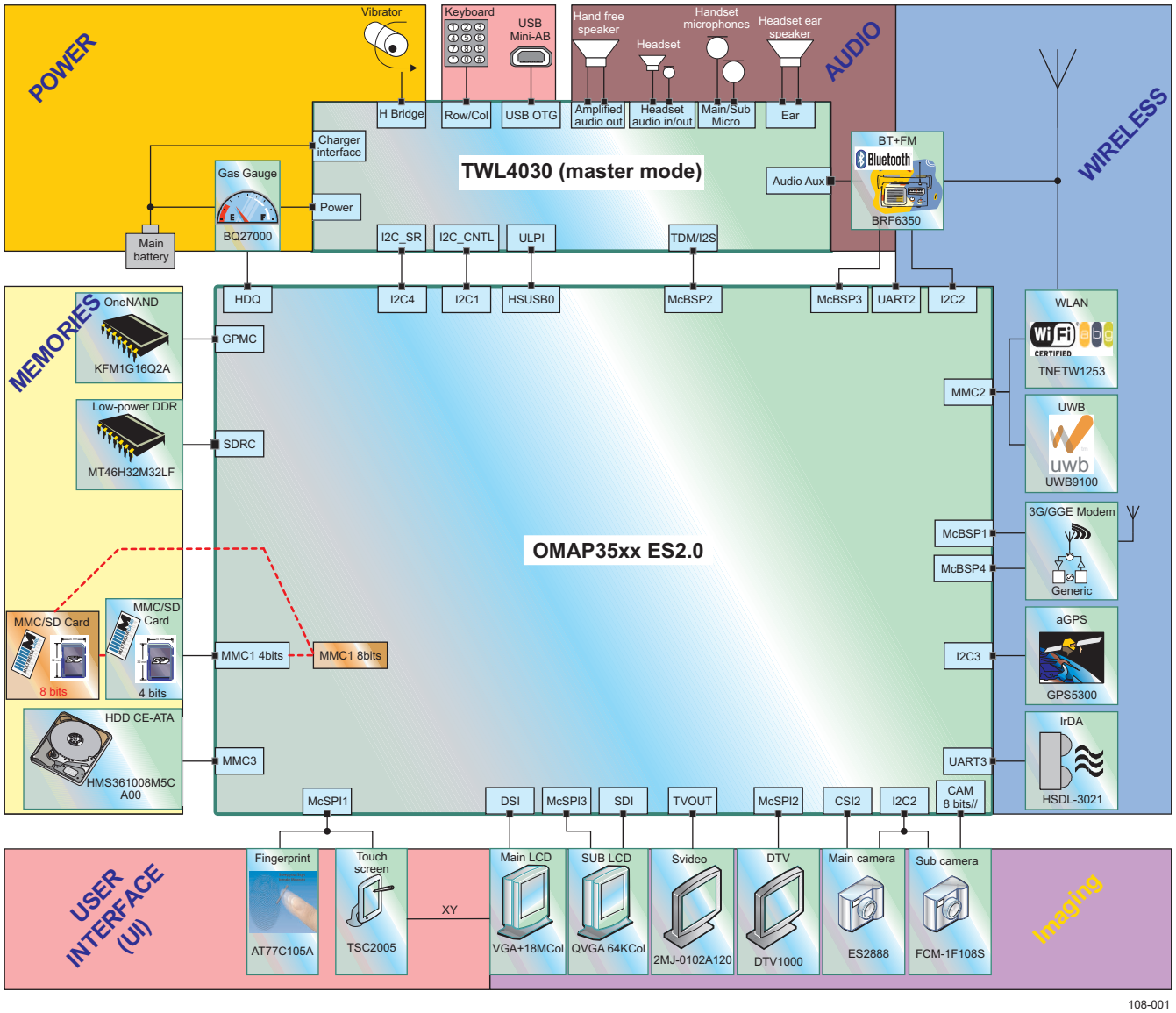
- A comprehensive power and clock-management scheme that enables high-performance, low-power operation, and ultralow-power standby features. The device also supports SmartReflex™ adaptative voltage control. This power management technique for automatic control of the operating voltage of a module reduces the active power consumption.
- A memory stacking feature using the package-on-package (POP) implementation (see Section 1.4, *Package-on-Package Concept*)

1.2 Environment

This section provides an overview of the OMAP environment. The device is associated with a power integrated circuit (IC). Texas Instruments provides a global solution with the TWL4030 device. For more information on the TWL4030 device, contact your TI representative.

Figure 1-1 provides an overview of a nonexhaustive environment for the high-tier OMAP35xx device.

Figure 1-1. OMAP35xx Environment Using TWL4030



108-001

Note: Some features are not available on all devices. See Section 1.5, *OMAP35xx Family*, for more information on available features.

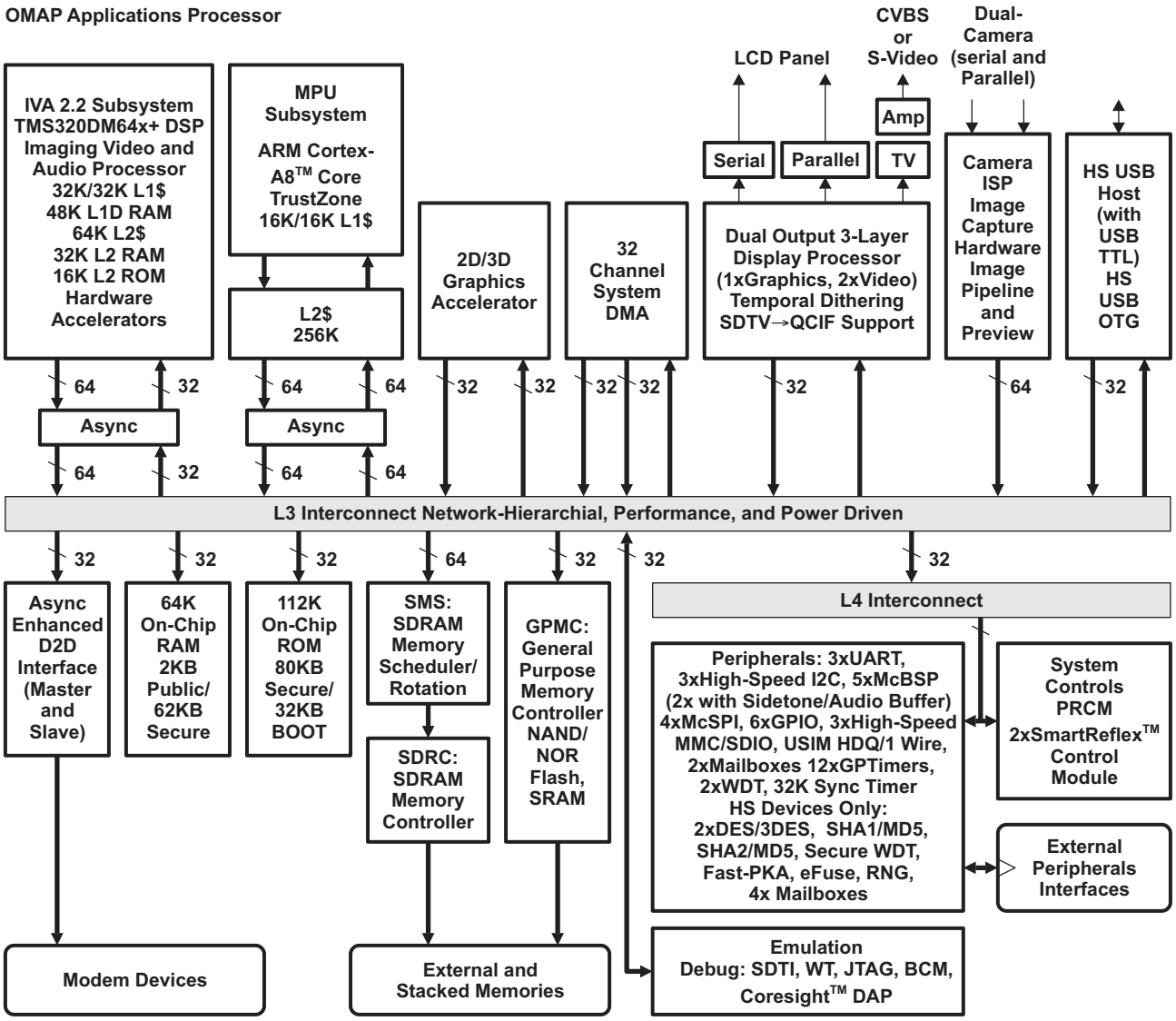
1.3 Description

The device is offered in two packages:

- CBB package: 515-ball, 12 x 12 mm, package-on-package (POP) 0.5-mm (top) and 0.4-mm (bottom) ball pitch package. Some balls are available at the top of the device to allow memory stacking. For more information, see Section 1.4, *Package-on-Package Concept*.
- CUS package: 423-ball, 16 x 16mm, 0.65-mm (bottom) ball pitch package

Figure 1-2 shows the block diagram.

Figure 1-2. Block Diagram



Note: Some features are not available on all devices. See Section 1.5, *OMAP35xx Family*, for more information on available features.

1.3.1 MPU Subsystem

The MPU subsystem integrates the following modules

- ARM subchip

  - ARM Cortex-A8 core
  - ARM Version 7™ ISA: Standard ARM instruction set + Thumb®-2, Jazelle® RCT Java accelerator, and media extensions
  - NEON™ SIMD coprocessor (VFP lite + media streaming instructions)
  - Cache memories
    - Level 1: 16KB instruction and 16KB data—4-way set associative cache, 64 bytes/line
    - Level 2: see Section 1.5, *OMAP35xx Family*.
- Interrupt controller (MPU IN TC) of 96 synchronous interrupt lines
- Asynchronous interface with core logic
- Debug, trace, and emulation features: ICE-Crusher, ETM, ETB modules.

1.3.2 IVA2.2 Subsystem

The device includes a high-performance imaging video and audio (IVA2.2) accelerator based on the Texas Instruments TMS320DMC64x+ VLIW DSP core.

The IVA2.2 subsystem includes the following main features:

- 32-bit fixed-point media processor
- Very long instruction word (VLIW) architecture based on the programmable enhanced version of C64x DSP core
- Eight instructions/cycle, eight execution units
  - Optimized instruction set for video and imaging processing
  - Eight 8 x 8 or 16 x 16 multiply accumulate (MAC) per cycle
  - Eight slave asynchronous die (SAD) per cycle
  - Eight interpolations (a + b + 1)>>1 per cycle
  - Two (32-bit x 32-bit > 64-bit) multiply operations per cycle
- Low-power processor and megacell
  - Dynamically mixed 32-bit and 16-bit instruction sets
  - Software pipelined loop (SPLOOP) instruction buffer
  - Separate power domain
  - Supported multiple power-down states
- Two-level memory subsystem hierarchy
  - L1P (program)
    - 32KB direct-mapped cache—32-byte cache line, configurable as cache or memory mapped (Possible values are: 0KB cache/32KB memory, 4KB/28KB, 8KB/24KB, 16KB/16KB, or 32KB/0KB)
  - L1D (data)
    - 32KB 2-way set associative cache—4-byte cache line, configurable as cache or memory mapped (Possible values are: 0KB cache/32KB memory, 4KB/28KB, 8KB/24KB, 16KB/16KB, or 32KB/0KB)
    - 48KB memory-mapped SRAM
  - L2 (program and data)
    - 64KB 4-way set associative cache—128-byte cache line, configurable as cache or memory mapped (Possible values are: 0KB cache/64KB memory, 32KB/32KB, or 64KB/0KB)
    - 32KB memory-mapped SRAM
    - 16KB ROM
- Video hardware accelerators
  - Improved motion estimation (iME) dedicated hardware
  - Improved loop filtering (iLF) dedicated hardware
  - Improved variable length coder/decoder (iVLCD) with quantizing capabilities dedicated hardware
  - Video dedicated sequencer
  - Video local interconnect

  - Local level 2 (L2) memory interface/arbiter
- Private direct memory access (DMA) controller:
  - 128 logical channels
  - 1D/2D addressing
  - Chaining capability
  - Fully pipelined, two 64-bit read ports, two 64-bit write ports
  - Single access 32-byte or 64-byte incrementing bursts
- Level 1 (L1) interrupt controller (INTC)
- Local IVA2.2 digital phase-locked loop (DPLL) supplying the IVA2.2 subsystem clocking
- 32-entry memory management unit (MMU) for seamless integration in high-level OS environment
- IVA2.2 system interfaces
  - 64-bit L3 port shared for external memory accesses
    - Multithreaded link shared by DSP core and DMA accesses
    - Interface with the L3 interconnect that can be synchronous or asynchronous for clock decoupling between IVA2.2 and L3 interconnect
    - Incrementing burst support
    - Critical line first to reduce line fetch latency to the processor
  - Host port interface (HPI) for MMU programming and access to the IVA2.2 internal memories. Can be synchronous or asynchronous
  - System interfaces: clocking, power management
- C-friendly environment (state-of-the-art C compiler for VLIW architecture)
- Texas Instruments low-overhead DSP-BIOS operating system

Note: IVA2.2 is not available on all devices. See Section 1.5, *OMAP35xx Family*, for more information on available features.

1.3.3 On-Chip Memory

On-chip memory configuration offers memory resources for program and data storage:

- 112KB ROM
- 64KB single-access static random access memory (SRAM)

1.3.4 External Memory Interfaces

The device includes two external memory interfaces supporting the stacking of a multichip memory package using the generic POP interface:

- General-purpose memory controller (GPMC)
  - NOR flash, NAND flash (with ECC Hamming code calculation), SRAM and Pseudo-SRAM asynchronous and synchronous protocols
  - Flexible asynchronous protocol control for external ASIC or peripheral interfacing
  - 16-bit data, up to 8 chip-selects (CSs)
  - 128M-byte addressable per chip-select, 1G-byte total address space
  - Nonmultiplexed device with limited address (2K bytes)
- SDRAM controller (SDRC)
  - Mobile single data rate (M-SDR) SDRAM and low-power double data rate (LPDDR) SDRAM
  - 16-bit or 32-bit data, 2 chip-selects, configurations for a maximum of 1 G-byte address space per chip-select
  - Work in conjunction with the SDRAM memory scheduler (SMS) companion module

1.3.5 DMA Controllers

The device embeds one generic DMA controller, the system DMA (sDMA) controller, used for memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers:

- One read port, one write port
- 32 prioritizable logical channels
- 96 hardware requests
- 256 x 32-bit FIFO dynamically allocable between active channels

The device also embeds three dedicated DMA controllers: enhanced DMA (EDMA), which is embedded in the IVA2.2 subsystem, display DMA, and USB HS DMA.

1.3.6 Multimedia Accelerators

The device uses the following multimedia accelerators for display and gaming effects as well as high-end imaging and video applications:

- 2D and 3D graphics accelerator (SGX or SGX530)
  - 2D and 3D graphics and video codecs supported on common hardware
  - Tile-based architecture
  - Universal scalable shader engine (USSE™) multithreaded engine incorporating pixel and vertex shader functionality reducing die area
  - Advanced shader feature set in excess of Microsoft VS3.0, PS3.0, and OGL2.0
  - Industry standard API support Direct3D mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0, OpenMax
  - Fine-grained task switching, load balancing, and power management
  - Programmable high-quality image anti-aliasing
  - Advanced geometry DMA driven operation for minimum CPU interaction
  - Fully virtualized memory addressing for OS operation in a unified memory architecture
  - Advanced and standard 2D operations (that is, vector graphics, BLTs, ROPs, etc.)
  - Programmable video encode and decode support for H.264, H.263, MPEG4 (SP), WMV9, and JPEG

Note: Multimedia accelerators are not available on all devices. See Section 1.5, *OMAP35xx Family*, for more information on available features.

- Camera interface
  - Supports most of the raw image sensors available in the market
  - Serial interface compatible with the CCP2/MIPI CSI1 specification (CSIb) and the MIPI CSI2 specification (CSIa)
  - Includes video processing hardware
  - 12-bit parallel interface supported
  - Pixel clock up to 83 MHz

CAUTION

Clock configurations depend on the core voltage and maximum clock frequencies. Values in this document might not apply to production devices. Refer to your device-specific data manual for supported values for production devices.

  - Embedded DMA controller in CSI2 receiver
- Display interface
  - Display controller
  - Color and monochrome displays up to 2048 x 2048 x 24-bpp resolution
  - 256 x 24-bit entries palette in red, green, blue (RGB)

- 3,375 colors, 15 grayscales
- Picture-in-picture (overlay), color-space conversion, rotation, color-phase rotation, and resizing support
- Remote frame buffer interface
- Liquid-crystal display (LCD) pixel interfaces (MIPI DPI 1.0) and LCD bus interfaces (MIPI DBI 1.0) supported
- NTSC/PAL video encoder outputs with integrated digital-to-analog converters (DACs) output are supported on CVBS and S-video TV analog output signals
- Serial display interface implements high-speed differential output buffers to support FlatLink3G™, Mobile CMADS and MIPI DSI 1.0 formats
- Embedded DMA controller

1.3.7 Security (HS Devices Only)

The secure firmware resides in a secure version of the ROM and includes hardware security features that enable HS devices and the following encryption/decryption accelerators:

- RNG
- 2 x DES/3DES
- SHA1/MD5
- SHA2/MD5
- 2 x AES with counter mode
- Fast PKA

The customer programmable fuse ROM (CPFROM) module is only available on high-security (HS) devices.

The universal subscriber identity module (USIM) that supports 3GPP extended features and EMV specific feature is available only on HS devices. This interface includes two modules: the fast-deactivate (FD) module and the USIM.

Note: This technical reference manual focuses only on general-purpose (GP) devices. To determine if a high-security (HS) version of your device is available and for more information on HS devices, see Section 1.5, *OMAP35xx Family*, and your device-specific data manual.

1.3.8 Comprehensive Power Management

OMAP35xx devices include the following power management features:

- Clock and reset generation and distribution
- Wake-up event management
- SmartReflex™ technology
- Dynamic voltage frequency shifting
- Dynamic power shifting
- Static leakage management

1.3.9 Peripherals

The device supports a comprehensive set of peripherals to provide flexible and high-speed interfacing and on-chip programming resources. Table 1-1 provides a list and description of the peripherals available on OMAP35xx devices.

Table 1-1. OMAP35xx Peripherals

Type	Name	Number	Description
Serial Communication	Multi-channel Buffered Serial Ports (McBSPs)	5	The McBSPs provide a full-duplex direct serial interface between the device and other devices in a system such as audio and voice codecs and other application chips. McBSP1, McBSP2, and McBSP3 serve as general purpose serial ports while McBSP2 and McBSP3 include additional audio-loopback capability.
	Multi-channel Serial Port Interface (McSPI)	4	The McSPIs provide a master/slave interface to SPI devices.
	High-speed Multi-port USB Host Controller	1	High-speed USB2.0 host controller with three host ports each offering high-speed data transactions (up to 480 Mbps) or full-speed/low-speed data transactions (12 and 1.5 Mbps, respectively). In high-speed mode, the USB host controller ports interface to external USB PHYs using a 12-pin or 8-pin UTMI low pin interface (ULPI). In full-speed and low-speed mode, the ports interface to external USB PHYs using a 6-/4-/3-pin serial interface. Additionally each port can be directly connected to a USB device (bypassing the need for USB PHY) by using an the on-chip transceiver-less link logic (TLL) adapter.
	High-speed USB OTG Controller	1	High-speed USB2.0 OTG controller that offers high-speed data transactions (up to 480 Mbps) on a USB port with embedded DMA controller. The high-speed USB OTG controller interfaces to an external USB PHY using a 12-pin UTMI low pin interface (ULPI).
	HDQ/1-Wire	1	The HDQ/1-Wire interface supports the Benchmark HDQ protocol and the Dallas Semiconductor 1-Wire protocol.
	Universal Asynchronous Receiver/Transmitter (UART)	3	Serial communication interfaces compatible to the industry standard TL16C550 asynchronous communications element. UART1 and UART 2 are general serial communication interfaces. UART3 provides additional support for infrared data association (IrDA) and consumer infrared (CIR) communications.
	High-speed (HS) Inter-integrated Circuit (I2C) Controllers	3 (1)	Master/slave I2C high-speed standard interfaces with support for standard mode (up to 100K bits/s), fast mode (up to 400K bits/s), and high-speed mode (up to 3.4M bits/s).
Removable Media	Multimedia Card/Secure Digital/Secure Digital I/O (MMC/SDIO) Card Interface	1	MMC memory card, SD memory card, or SDIO cards interface.
Miscellaneous	GP timers	12	Twelve general-purpose timers
	Watchdog timers (WDTs)	2	Three watchdog timers
	32-kHz synchronization timer	1	32-kHz clock timer
	General-purpose input/output (GPIO)	Package-specific	General-purpose input/output pins controlled by six GPIO controllers.
	Mailbox	6	MPU/IVA2.2 inter-processor communications mailboxes. All six mailboxes are available in chassis mode, however, only two mailboxes are available in stand-alone mode.
	Control module	1	I/O multiplexing and chip-configuration control.
Security Modules (High-security Devices Only)			RNG, Fast PKA, 2xDES/3DES, SHA1/MD5, SHA2/MD5, 2xAES, Secure Watchdog Timer, and universal subscriber identity module (USIM).

(1) A fourth master/transmitter high-speed I2C interface (I2C4) is included in the power, reset, and clock management (PRCM) module to perform dynamic voltage control and power sequencing.

1.4 Package-On-Package Concept

The OMAP35xx CBB package provides a package-on-package (POP) memory interface to support multiple stacked package configurations, including a flash multi-chip package, depending on customer needs. Note that use of standalone memory devices is also possible on the CBB package; use of POP technology is not required.

The stacked memory package is directly connected to the two memory interfaces (GPMC and SDRC) of the OMAP35xx CBB package through the POP interface present at the top. For more information on the interconnect between the stacked memory package and the OMAP35xx CBB package, see Chapter 11, Memory Subsystem, and your device-specific OMAP35xx data manual.

Note: Before using the POP memory interface, a compatible memory device supply must first be secured directly from specific memory vendors.

Figure 1-3 shows the concept of the POP solution, and Figure 1-4 shows stacked memory package on the POP device.

Figure 1-3. POP Concept (CBB Package)

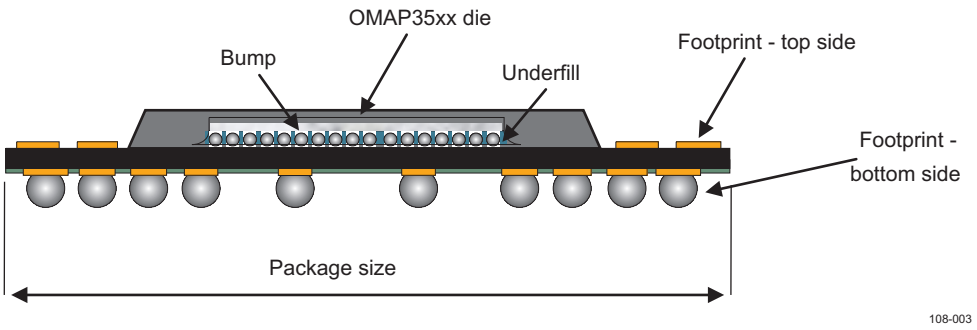
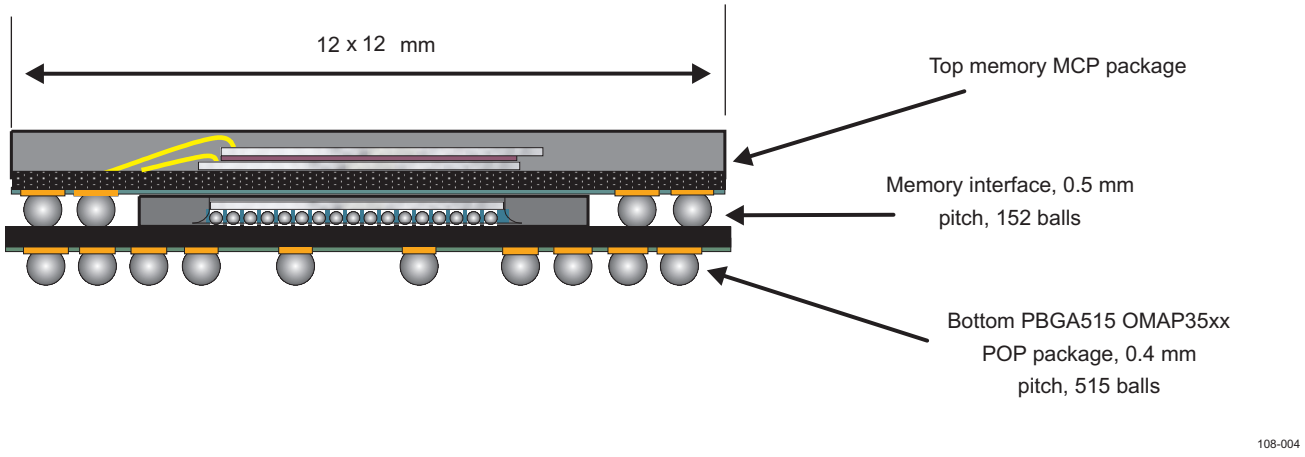


Figure 1-4. Stacked Memory Package on the POP Device (CBB Package)



The memory interfaces should be correctly configured based on the memory package used with the POP device.

Table 1-2 summarizes the supported configurations with the generic POP interface.

Note: Use of standalone memory devices is also possible on the CBB package; use of POP technology is not required.

Table 1-2. Summary of Memories Supported by the POP Interface

Generic POP Interface Features Set	SDRC Interface	GPMC Interface
Type of memory supported	MDDR	NOR flash asynchronous and synchronous burst flash NAND flash "CE don't care" One NAND on CS0 and CS1 NOR flash address/data nonmultiplexed is not supported.
Number of chip-selects	2	2
Maximum density per chip-select	1G bit	512M bits (NOR flash) or 4G bits NAND flash
Maximum size per interface	2G bits	1G bit (NOR flash) or 8G bits NAND flash
Interface width	X 32 bits	X 16 bits
I/O voltage	1.8 V LVCMOS	1.8 V LVCMOS

For more information on the memory interface configuration, see the *Memory Subsystem* chapter.

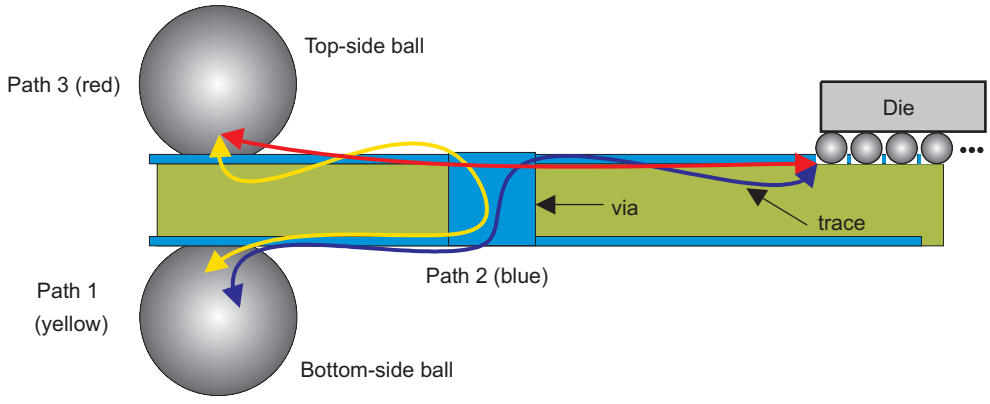
The POP device includes feedthroughs in addition to the GPMC and SDRC interfaces positioned at the top of the package. Up to 47 feedthroughs are defined from the bottom ball-grid array (BGA) to the top (or POP) interface to support different memory combinations.

The feedthroughs either provide power to a top memory device or provide specific memory signals (for example, control and/or address signals) from the bottom BGA to the POP interface.

Note: It is possible to monitor the DDR SDRAM temperature if the memory multichip package allows the temperature sensing option. A feedthrough is used to lower the temperature sensing dedicated signal to make a connection with a GPIO. For more information on DDR SDRAM temperature sensing management, see the *Memory Subsystem* and the *General-Purpose Interface* chapters.

Figure 1-5 shows the implementation of feedthroughs on the POP and the different paths between the bottom and the top of the package.

Figure 1-5. Stacked Memory Package on the POP Device (CBB Package)



(1) Path 1: feedthrough only; Path 2: all but feedthrough; Path 3: POP interface (SDRC + subset GPMC)

(2) Any signal available on the POP interface to a top-side ball is also available to a bottom-side ball.

1.5 OMAP35xx Family

1.5.1 Device Features

The OMAP 3 architecture is configured with different sets of features in different devices. This technical reference manual details all of the features available in current and future OMAP35xx devices. Some features may not be available or supported in your particular device. The features supported across different OMAP35xx devices are shown on Table 1-3 (CBB package) and Table 1-4 (CUS package). For more information on the CBB and CUS package refer to your device-specific data manual.

Table 1-3. Subsystem, Co-Processor, and Peripheral Support on OMAP35xx Devices (CBB Package)

Subsystem/Co-Processor/Peripheral	Chapter	OMAP3530	OMAP3525	OMAP3515	OMAP3503
IVA2.2 Subsystem	14	ü	ü		
2D/3D Graphics Accelerator	13	ü		ü	
Cortex-A8 Neon Co-Processor	3	ü	ü	ü	ü
SDRAM Controller	11	ü	ü	ü	ü
General-Purpose Memory Controller	11	ü	ü	ü	ü
Package-on-Package	1	ü	ü	ü	ü
Chassis Mode	1				
Intersystem Communication Registers (ICRs)					
Modem Interrupt Controller Registers					
Four Mailboxes					
Slave Die-to-Die (SAD2D)					
Module Master Die-to-Die (MAD2D)					
Module SMX Firewall for Asynchronous Die-to-Die (AD2D)					
Camera ISP	12	ü	ü	ü	ü
Camera Serial Interface 1 (CSI1)					
Camera Serial Interface 2 (CSI2)					
Display Subsystem	15	ü	ü	ü	ü
LCD and TV Output Interface		ü	ü	ü	ü
Serial Display Interface (SDI)					
Display Serial Interface (DSI)					
McBSP1/2/3/4/5	22	ü	ü	ü	ü
McSPI1/2/3/4	20	ü	ü	ü	ü
High-Speed USB OTG Controller	25	ü	ü	ü	ü
High-Speed USB Host Controller	25	ü	ü	ü	ü
HDQ/1-Wire	21	ü	ü	ü	ü
UART1/2	18	ü	ü	ü	ü
UART3/IrDA/CIR	18	ü	ü	ü	ü
I2C1/2/3	19	ü	ü	ü	ü
MMC/SD/SDIO1/2/3	23	ü	ü	ü	ü
GP Timer (x12)	26	ü	ü	ü	ü
Watchdog Timer (x2)	26	ü	ü	ü	ü
32-kHz Sync Timer	26	ü	ü	ü	ü
GPIO	26	ü	ü	ü	ü

Table 1-3. Subsystem, Co-Processor, and Peripheral Support on OMAP35xx Devices (CBB Package) (continued)

Subsystem/Co-Processor/Peripheral	Chapter	OMAP3530	OMAP3525	OMAP3515	OMAP3503
Secure ROM	1				
RNG	1				
DES/3DES	1				
SHA1/MD5	1				
SHA2/MD5	1				
AES	1				
Fast PKA	1				
Secure Watchdog Timer	1				
Universal Subscriber Identify Module	1				
High-security Device	1				
General-purpose Device	1	ü	ü	ü	ü

Table 1-4. Subsystem, Co-Processor, and Peripheral Support on OMAP35xx Devices (CUS Package)

Subsystem/Co-Processor/Peripheral	Chapter	OMAP3530	OMAP3525	OMAP3515	OMAP3503
IVA2.2 Subsystem	14	ü	ü		
2D/3D Graphics Accelerator	13	ü		ü	
Cortex-A8 Neon Co-Processor	3	ü	ü	ü	ü
SDRAM Controller	11	ü	ü	ü	ü
General-Purpose Memory Controller (1)	11	ü	ü	ü	ü
Package-on-Package	1				
Chassis Mode	1				
Intersystem Communication Registers (ICRs)					
Modem Interrupt Controller Registers					
Four Mailboxes					
Slave Die-to-Die (SAD2D)					
Module Master Die-to-Die (MAD2D)					
Module SMX Firewall for Asynchronous Die-to-Die (AD2D)					
Camera ISP	12	ü	ü	ü	ü
Camera Serial Interface 1 (CSI1)					
Camera Serial Interface 2 (CSI2)					
Display Subsystem	15	ü	ü	ü	ü
LCD and TV Output Interface		ü	ü	ü	ü
Serial Display Interface (SDI)					
Display Serial Interface (DSI)					
McBSP1/2/3/4/5	22	ü	ü	ü	ü
McSPI1/2/3/4 (2)	20	ü	ü	ü	ü
High-Speed USB OTG Controller	25	ü	ü	ü	ü
High-Speed USB Host Controller (3)	25	ü	ü	ü	ü
HDQ/1-Wire	21	ü	ü	ü	ü

(1) Chip select pins gpmc_ncs1 and gpmc_ncs2 as well as wait pins gpmc_wait1 and gpmc_wait2 are not available on the CUS package.
(2) Chip select pins mcspi1_cs1 and mcspi_cs2 are not available on the CUS package.
(3) High-speed USB host controller port 3 is not available on the CUS package.

Table 1-4. Subsystem, Co-Processor, and Peripheral Support on OMAP35xx Devices (CUS Package) (continued)

Subsystem/Co-Processor/Peripheral	Chapter	OMAP3530	OMAP3525	OMAP3515	OMAP3503
UART1/2 (4)	18	ü	ü	ü	ü
UART3/IrDA/CIR	18	ü	ü	ü	ü
I2C1/2/3	19	ü	ü	ü	ü
MMC/SD/SDIO1/2/3	23	ü	ü	ü	ü
GP Timer (x12)	26	ü	ü	ü	ü
Watchdog Timer (x2)	26	ü	ü	ü	ü
32-kHz Sync Timer	26	ü	ü	ü	ü
GPIO (4)	26	ü	ü	ü	ü
Secure ROM	1				
RNG	1				
DES/3DES	1				
SHA1/MD5	1				
SHA2/MD5	1				
AES	1				
Fast PKA	1				
Secure Watchdog Timer	1				
Universal Subscriber Identify Module	1				
High-security Device	1				
General-purpose Device	1	ü	ü	ü	ü

(4) A maximum of 170 GPIO pins are supported. The following GPIO pins are not available: gpio_52, gpio_53, gpio_63 gpio_64, gpio_144, gpio_145, gpio_146, gpio_147, gpio_152, gpio_153, gpio_154, gpio_155, gpio_175, and gpio_176. Pin muxing restricts the total number of GPIO pins available at one time. See your device-specific data manual for more information on pin multiplexing.

1.5.2 Device Identification

The identification registers include the CONTROL_IDCODE and CONTROL_DIE_ID data registers. These registers are accessible through the L4 interconnect port starting at physical address 0x4830 A204 and 0x4830 A218, respectively. See the Memory Mapping chapter for more information about the L4 memory space mapping. Table 1-5 and Table 1-9 describe the identification registers.

The silicon type can be read in the HAWKEYE bit field value of the CONTROL.CONTROL_IDCODE register. The silicon revision can be read in the VERSION bit field value of the CONTROL.CONTROL_IDCODE register.

Table 1-5. Device Identification Registers

Register Name	Address	Size
CONTROL.CONTROL_IDCODE[31:0]	0x4830 A204	32
CONTROL.CONTROL_DIE_ID[127:0]	0x4830 A218	128

Table 1-6. CONTROL_IDCODE Register Definition

Field	Bits	Value	Comment
CONTROL.CONTROL_IDCODE [31:28]	VERSION	See Table 1-8.	Revision number
CONTROL.CONTROL_IDCODE [27:12]	HAWKEYE	See Table 1-7.	Hawkeye number

Table 1-6. CONTROL_IDCODE Register Definition (continued)

Field	Bits	Value	Comment
CONTROL.CONTROL_IDCODE [11:1]	TI_IDM	0x13	Manufacturer identity (TI)
CONTROL.CONTROL_IDCODE [0]	--	0x1	Always set to 1.

The Hawkeye number is hardcoded in the design. Table 1-7 lists the Hawkeye number values, and Table 1-8 lists the revision number values.

Table 1-7. Hawkeye Number Value

Silicon Type	Field	Value
OMAP35xx ES2.0	CONTROL.CONTROL_IDCODE[27:12]	0xB7AE
OMAP35xx ES2.1	CONTROL.CONTROL_IDCODE[27:12]	0xB7AE

Table 1-8. Revision Number Value

Silicon Type	Field	Value
ES 2.0	CONTROL.CONTROL_IDCODE[31:28]	0000
ES 2.1	CONTROL.CONTROL_IDCODE[31:28]	0001

The CONTROL.CONTROL_IDCODE value is 0x0B7A E02F for OMAP35xx ES2.0.

The CONTROL.CONTROL_IDCODE value is 0x1B7A E02F for OMAP35xx ES2.1.

The CONTROL.CONTROL_DIE_ID register is the 128 bits single identifier of the device.

Table 1-9. CONTROL_DIE_ID

Field	Bits	Value
DIE_ID[127:0]	RESERVED	Single identifier

1.5.3 General Recommendations Relative to Unavailable Features/Modules

As explained in the previous section, some features are not available in all OMAP35xx devices. For unavailable features, use the following recommendations:

- Memory mapping: Memory area of unavailable modules and features are RESERVED, read is undefined, and write can lead to unpredictable behavior.
- Interrupt controllers: Ensure that interrupts of unavailable modules and features are masked in MPU/IVA subsystems.
- DMA: Ensure that DMA requests of unavailable modules and features are masked in DMA subsystems.
- System Control Module (SCM): Unavailable modules and feature pins are not functional and should not be used.
- Power, Reset, and Clock Management Module (PRCM): For power management and power-saving consideration, ensure that power domains of unavailable features/modules are switched off and clocks are cut off.
- Interconnect: To flag potential interconnect outstanding commands, the time-out of target agents attached to unavailable modules can be enabled with the lowest setting.

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